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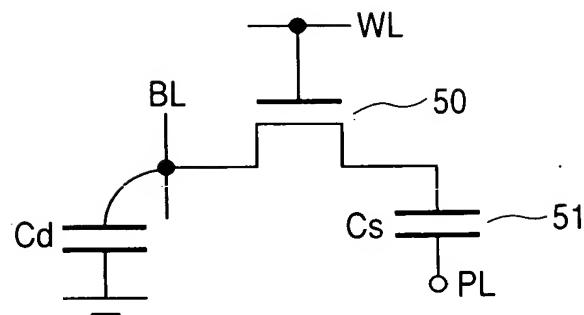
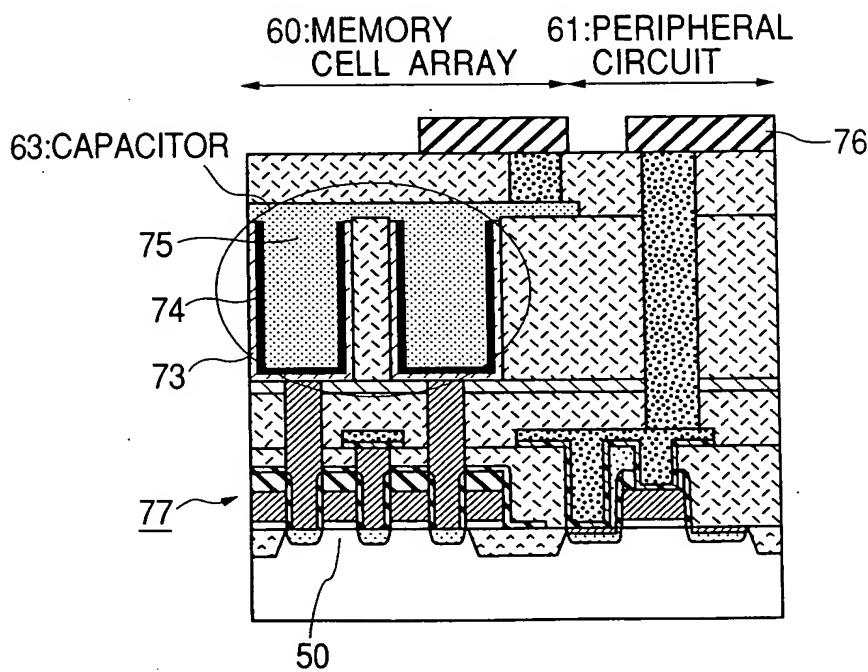
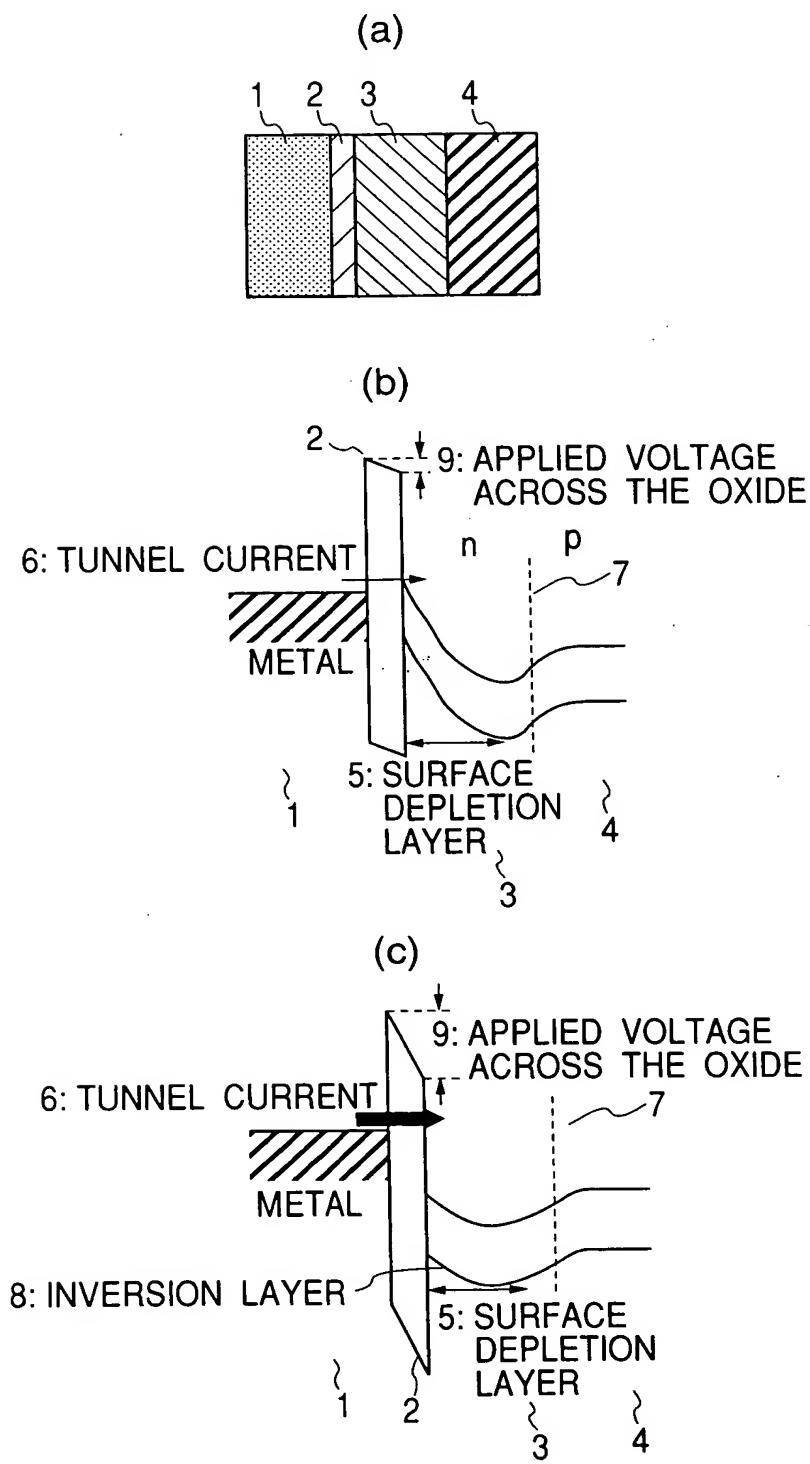
**FIG. 1****FIG. 2**

FIG. 3



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FIG. 4

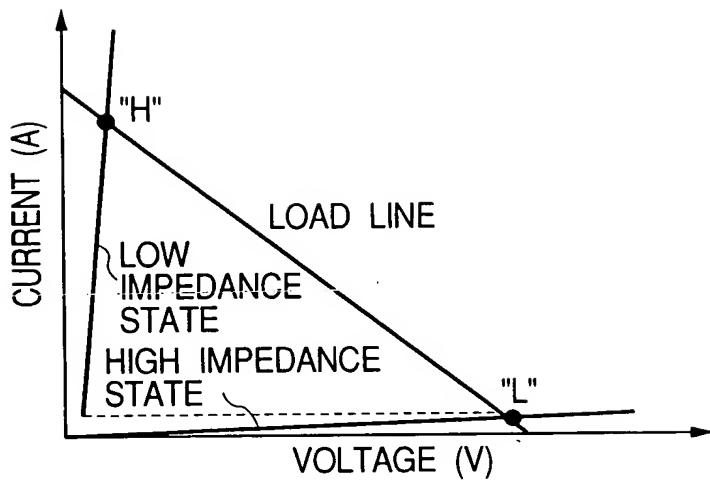


FIG. 5

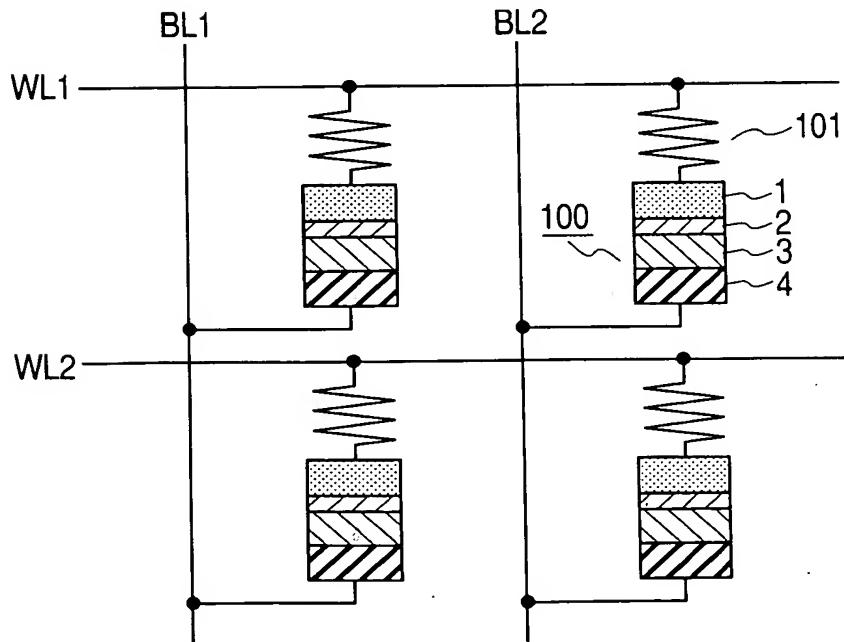
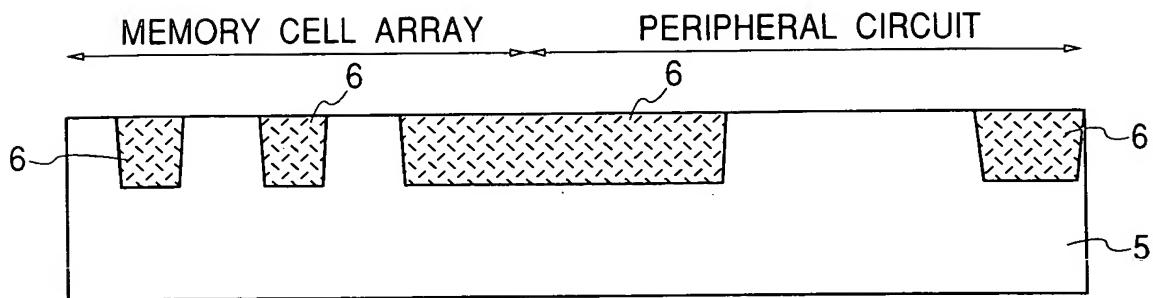


FIG. 6

(a)



(b)

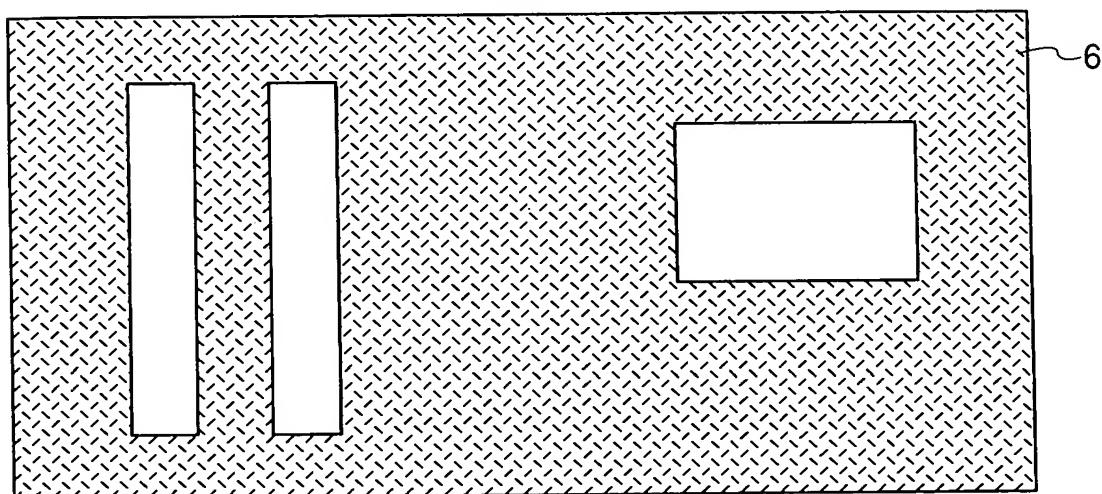


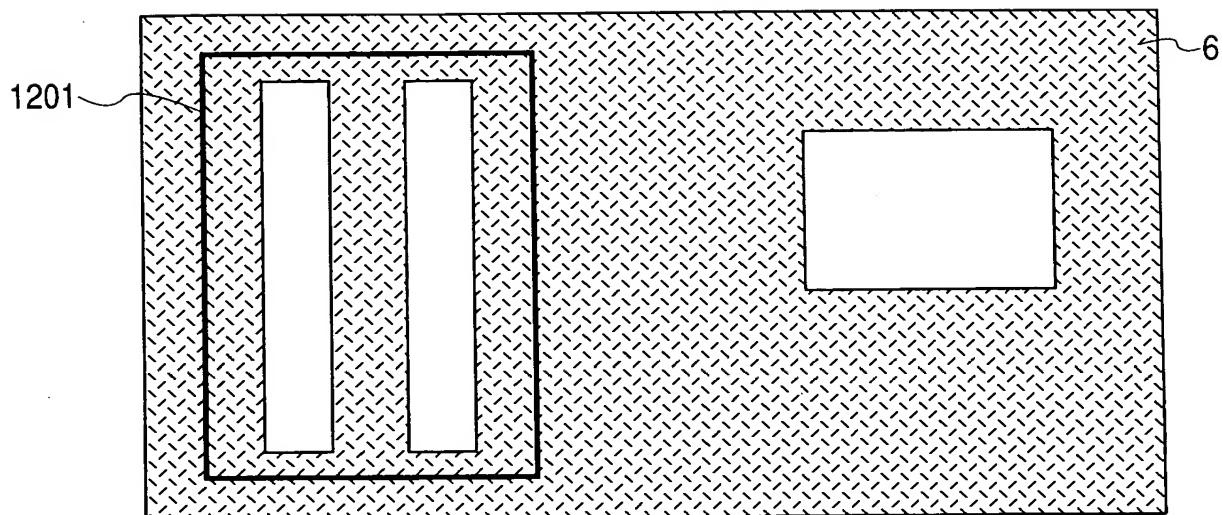
FIG. 7

The diagram illustrates a cross-sectional view of a memory cell array structure. At the top, two horizontal arrows point in opposite directions, labeled "MEMORY CELL ARRAY" on the left and "PERIPHERAL CIRCUIT" on the right. Below these labels, a thick horizontal line represents the substrate. The substrate is divided into several regions: four rectangular blocks labeled "6" at their top edges, a large rectangular block labeled "6" at its top edge, and a long rectangular block labeled "5" at its bottom edge. The region labeled "6" consists of a hatched pattern of small squares. The region labeled "7" is a solid gray rectangle positioned below the first four blocks. A vertical line on the right side of the diagram is labeled "6" at its top and "5" at its bottom, indicating a boundary between the array and the peripheral circuit.

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*FIG. 8*

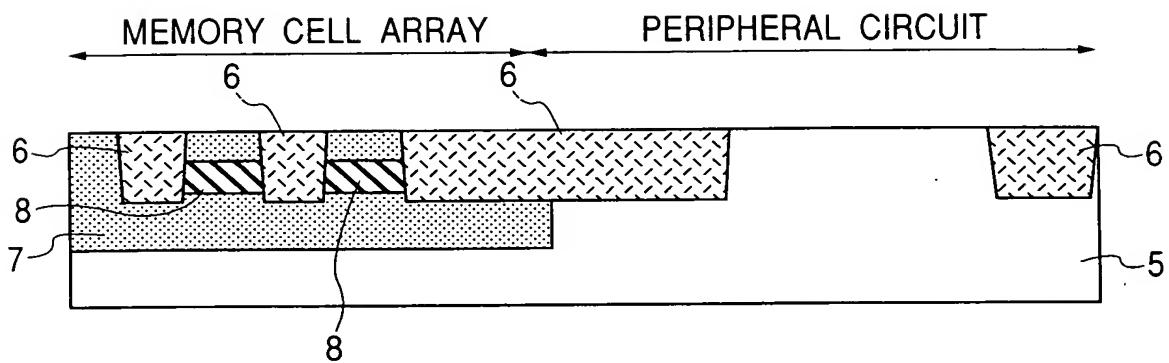
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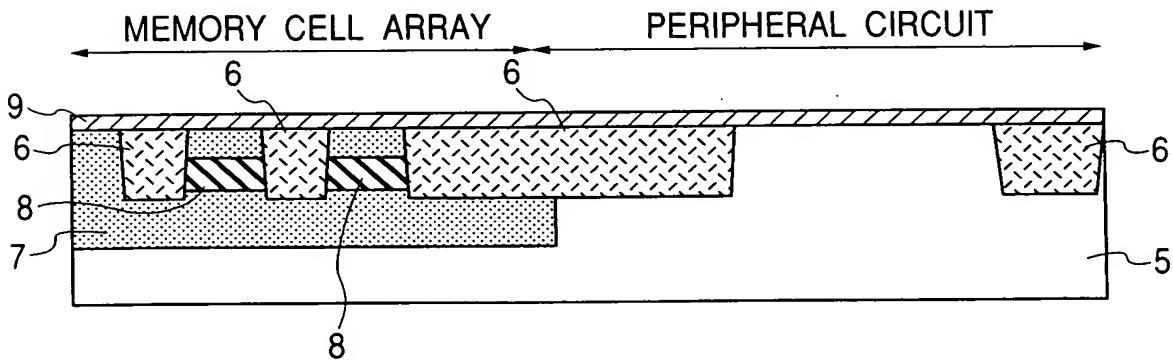
10/009826

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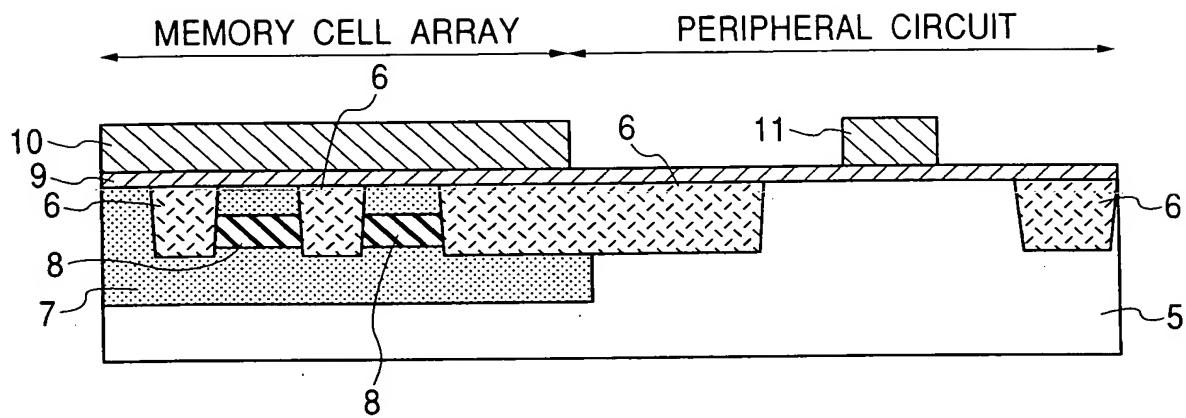
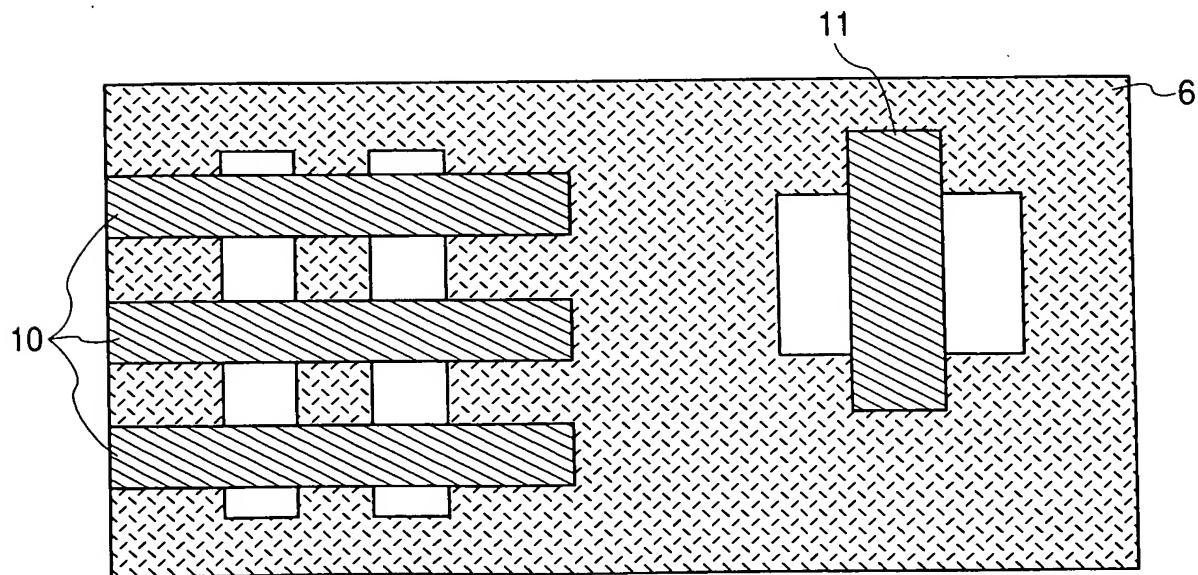
**FIG. 9**



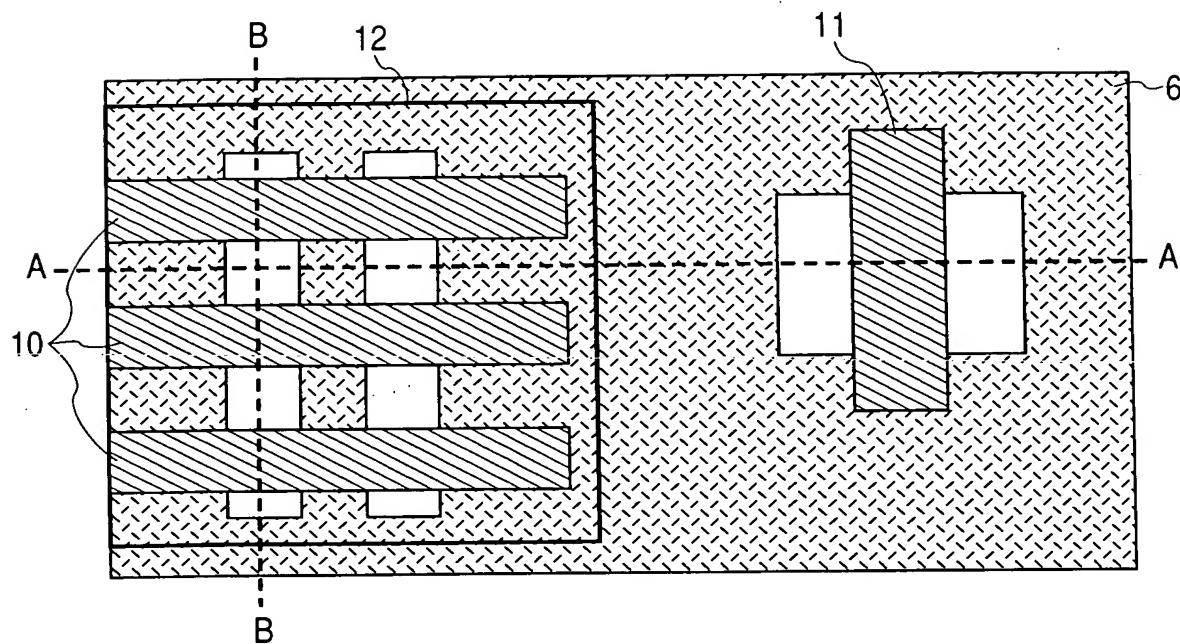
*FIG. 10*



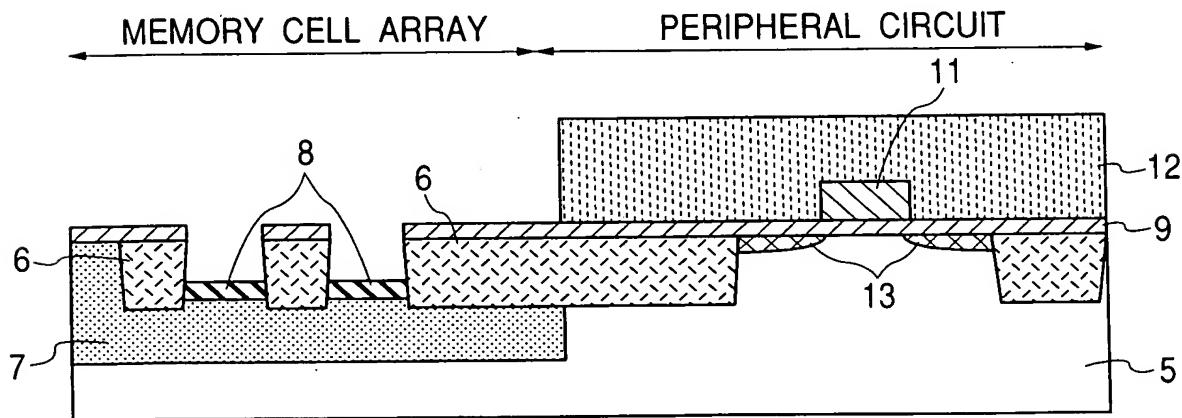
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**FIG. 11****FIG. 12**

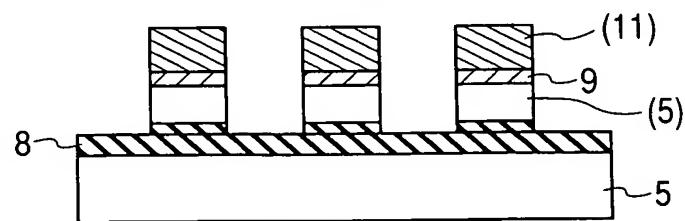
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**FIG. 13****FIG. 14**

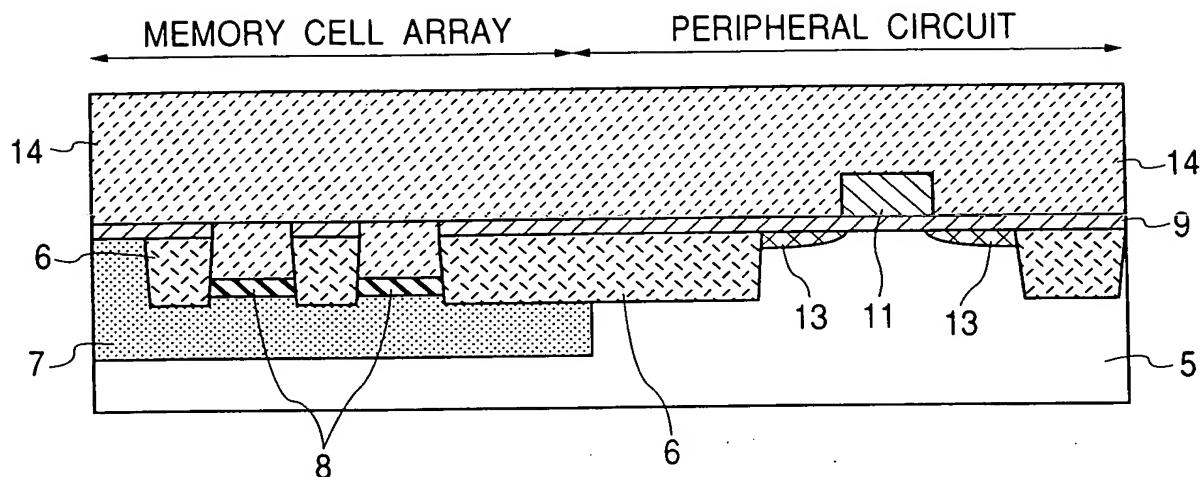
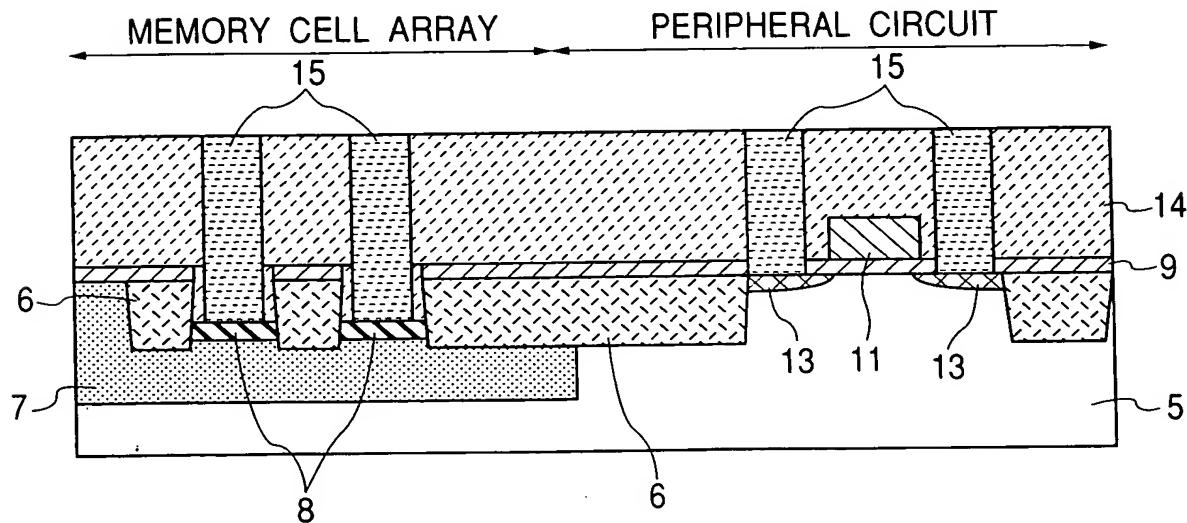
(a)



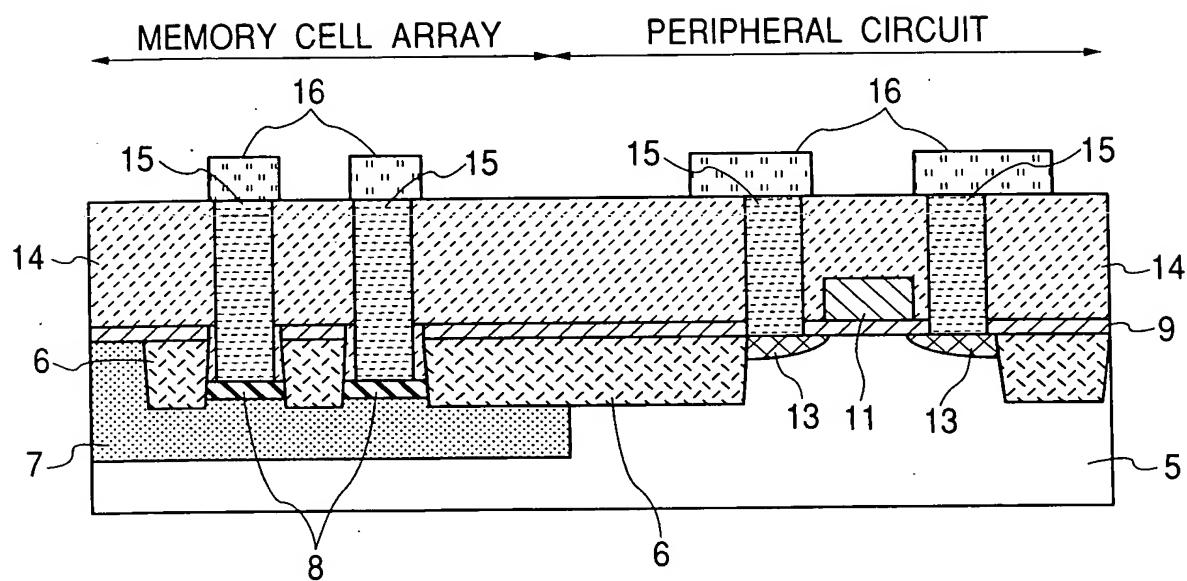
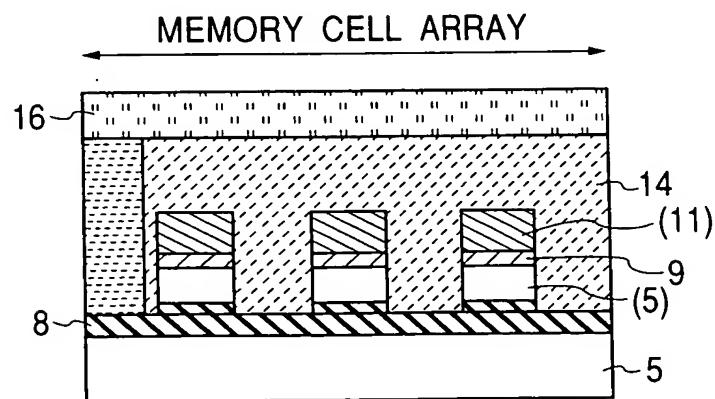
(b)



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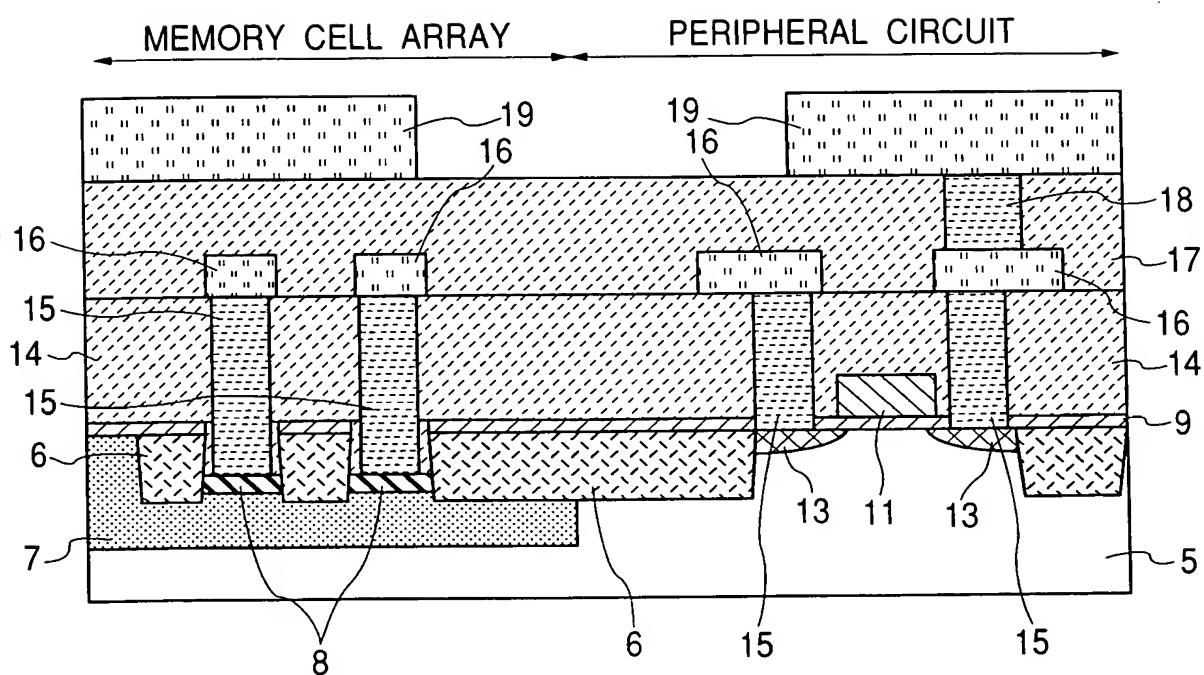
***FIG. 15******FIG. 16***

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***FIG. 17******FIG. 18***

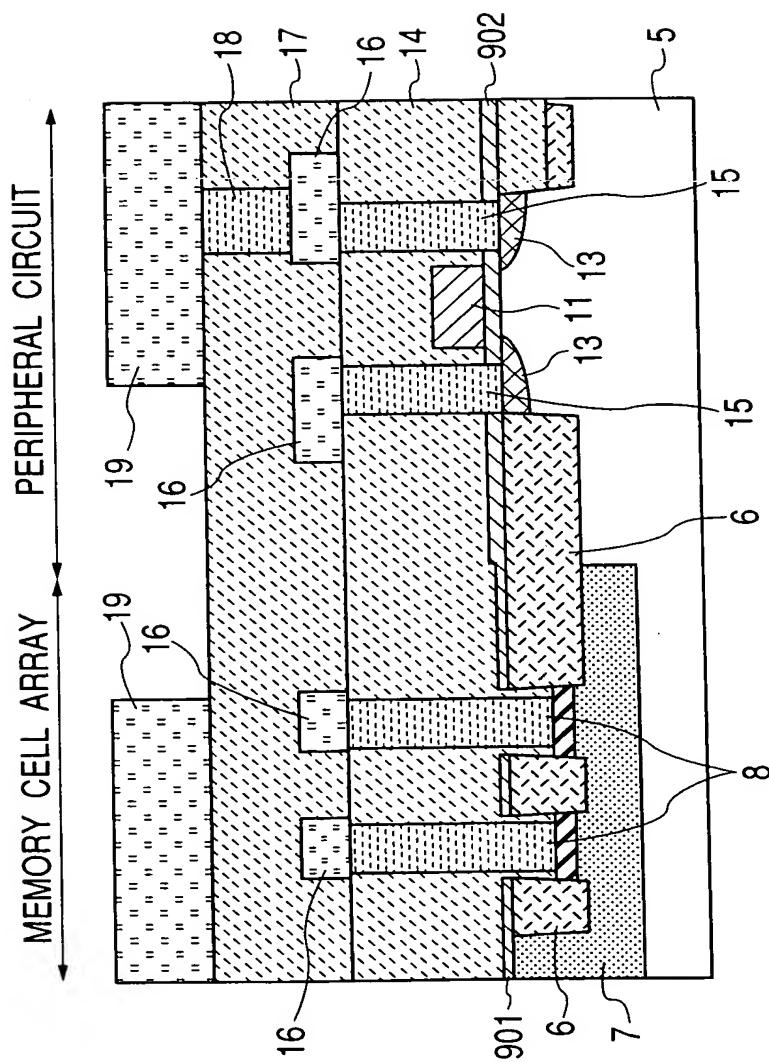
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FIG. 19



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FIG. 20



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FIG. 21

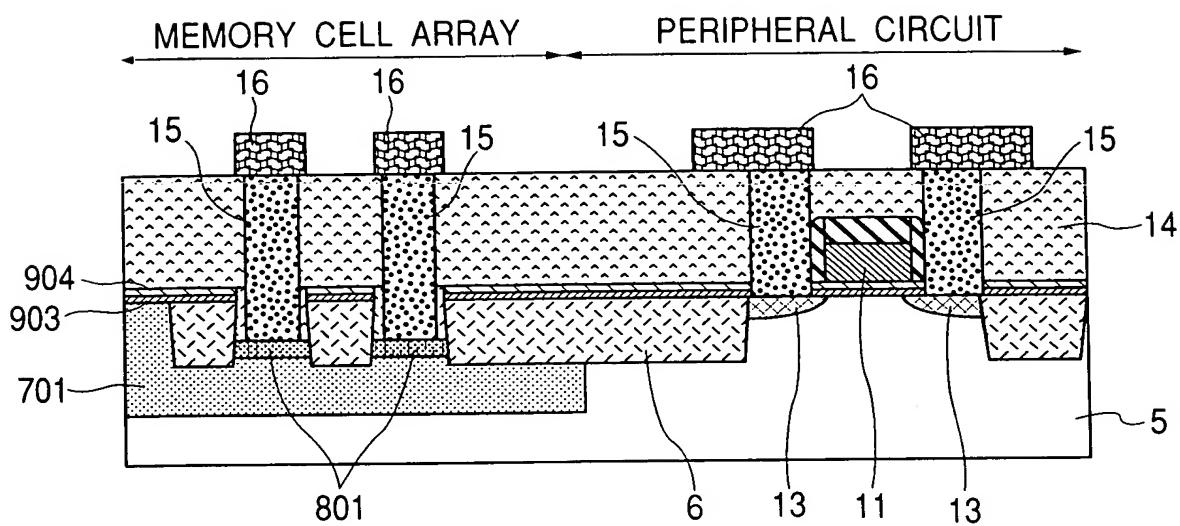
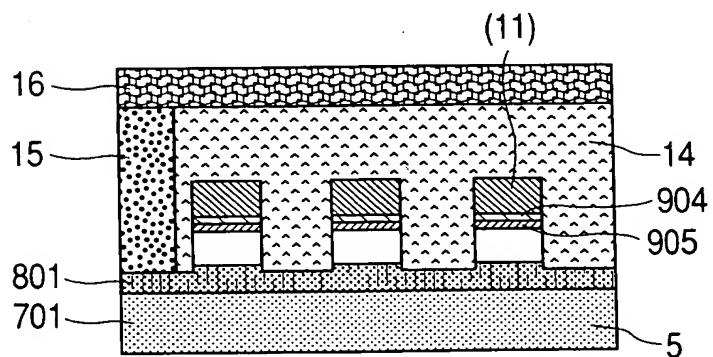
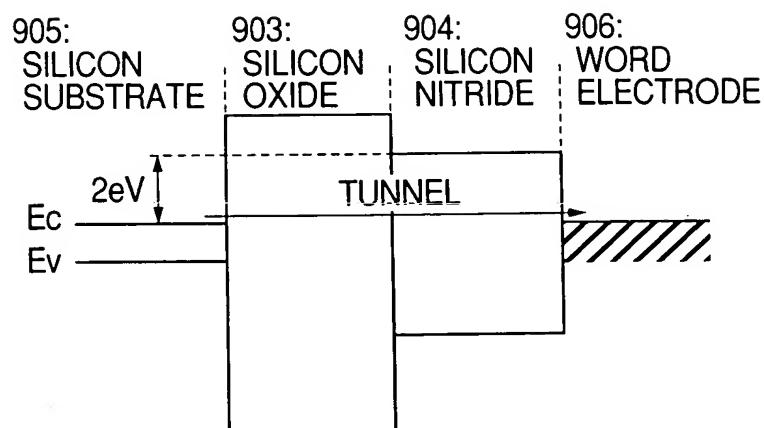
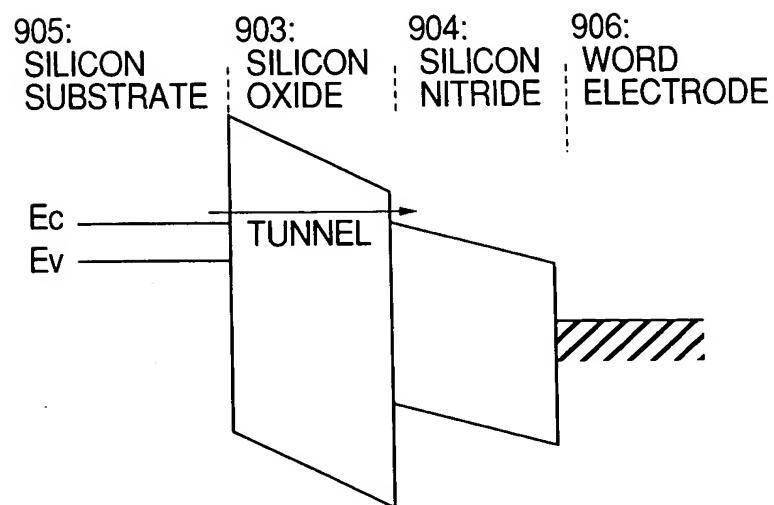


FIG. 22



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***FIG. 23******FIG. 24***

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FIG. 25

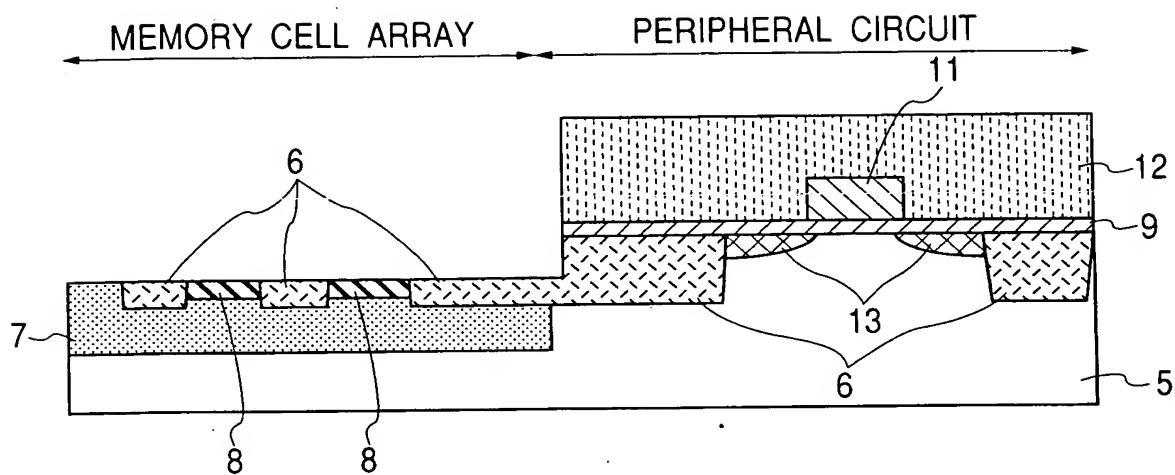
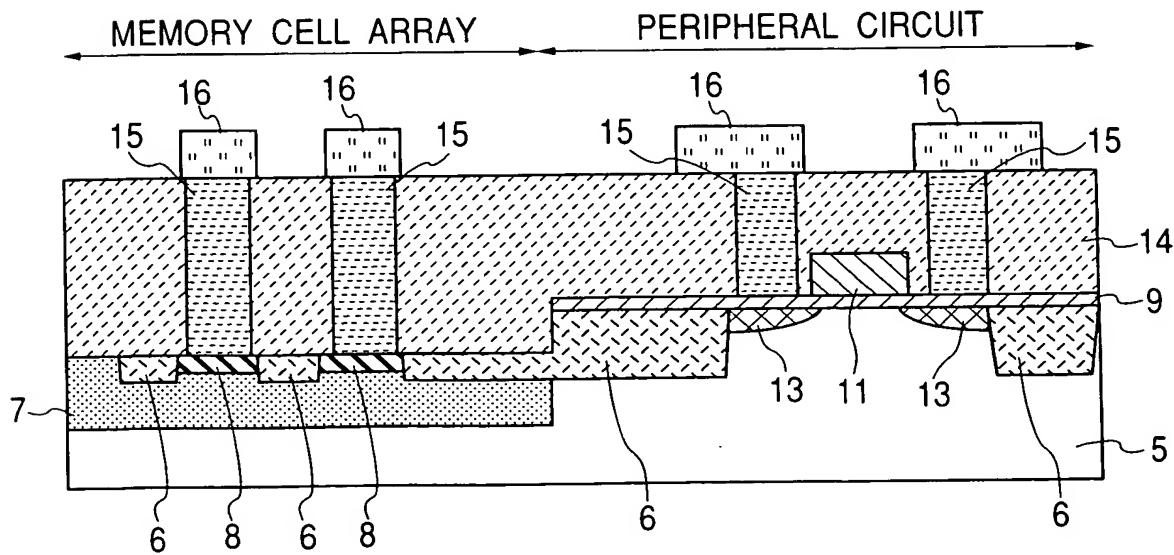
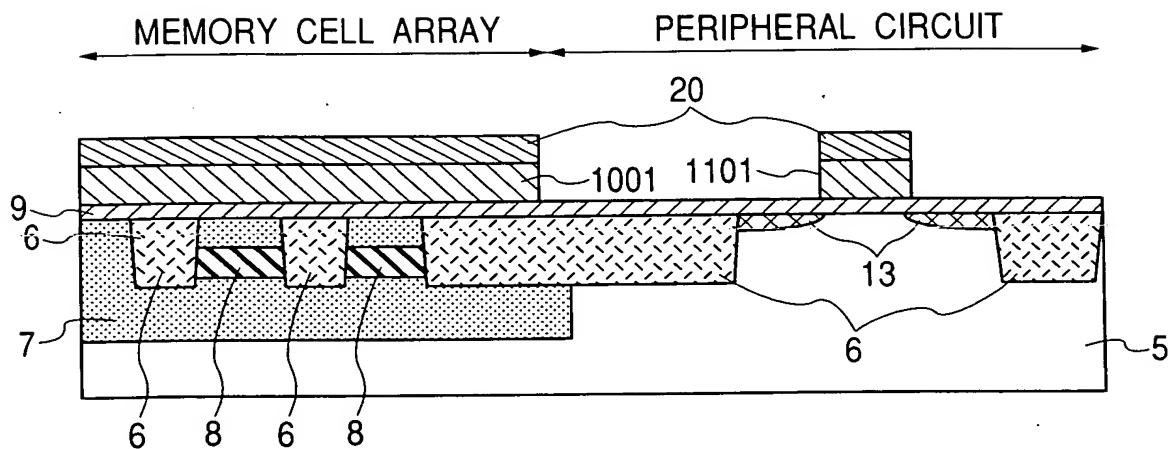
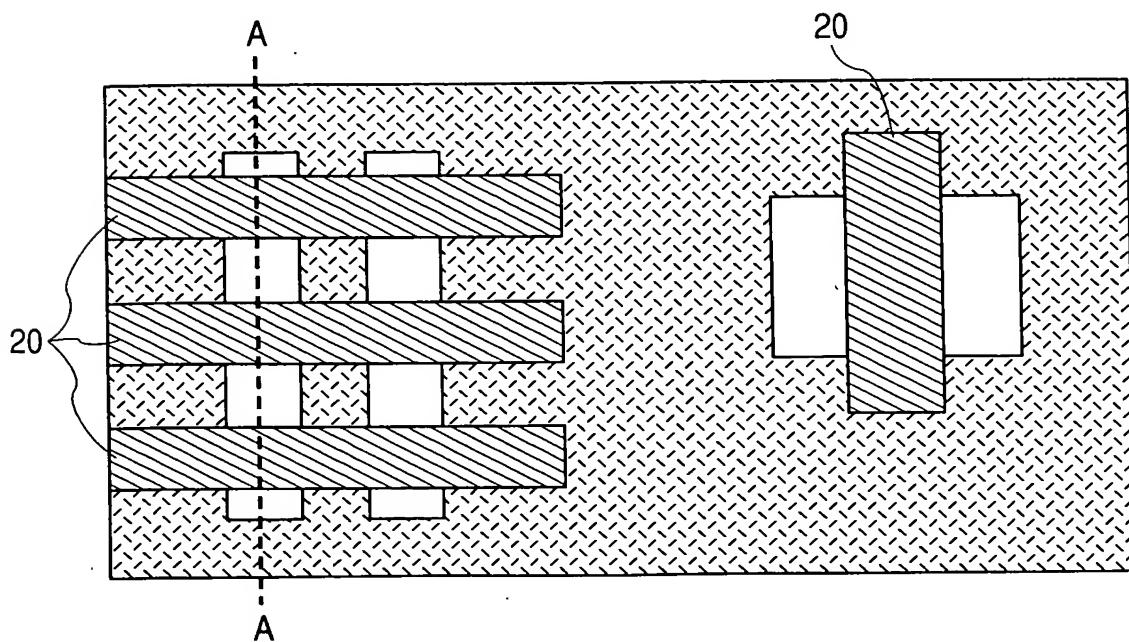


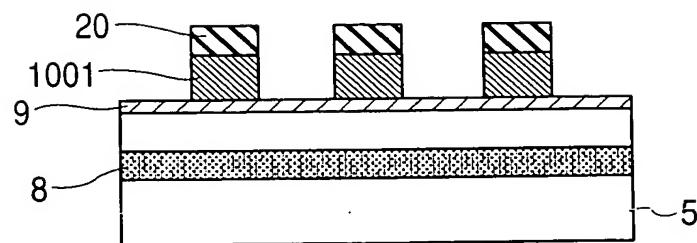
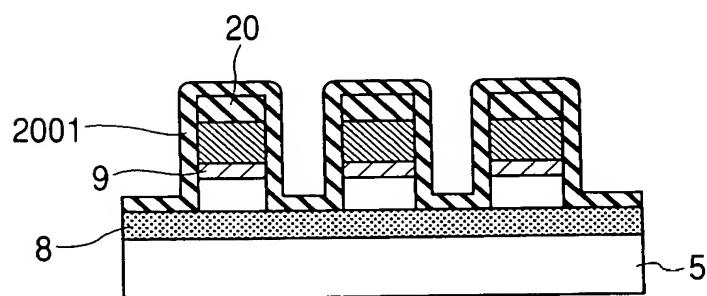
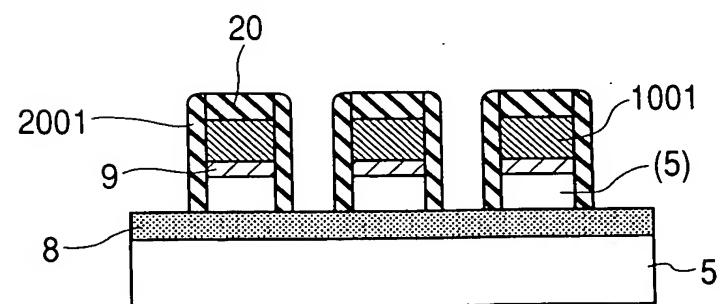
FIG. 26



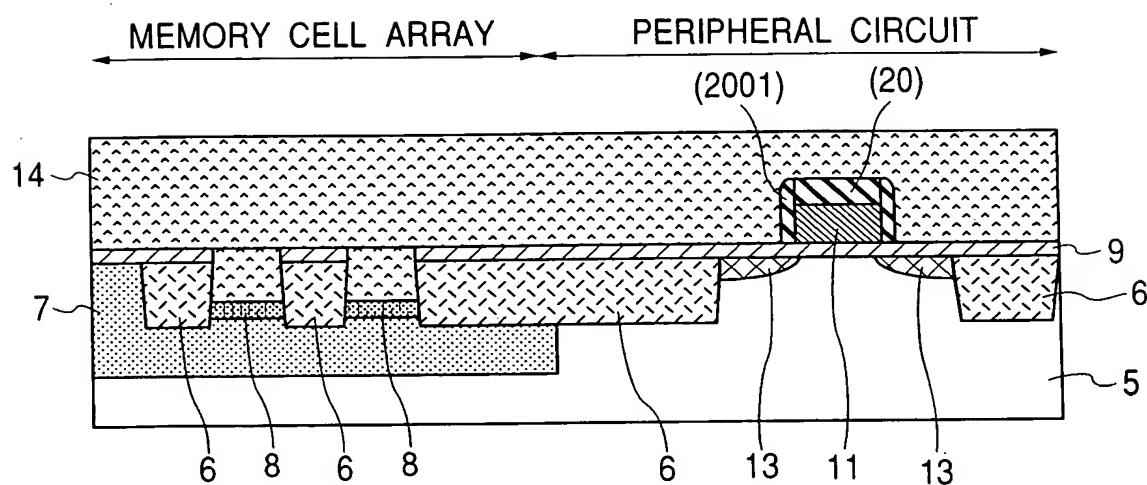
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**FIG. 27****FIG. 28**

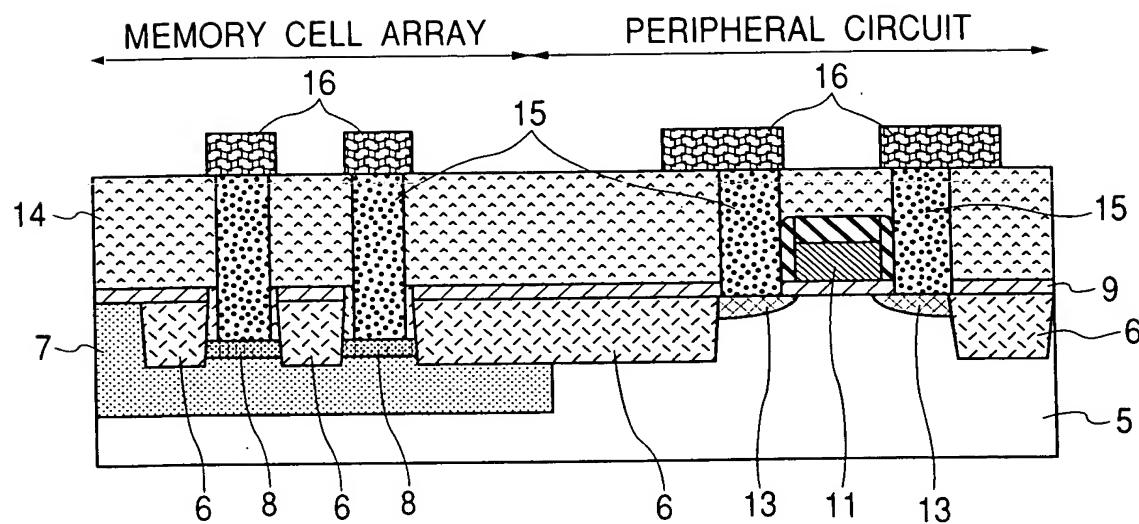
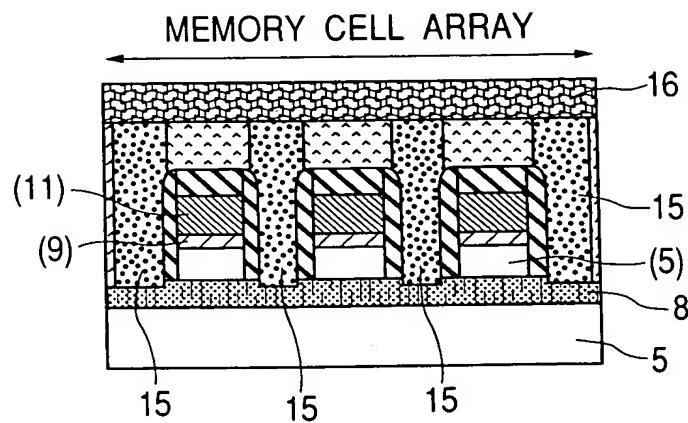
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*FIG. 29**FIG. 30**FIG. 31*

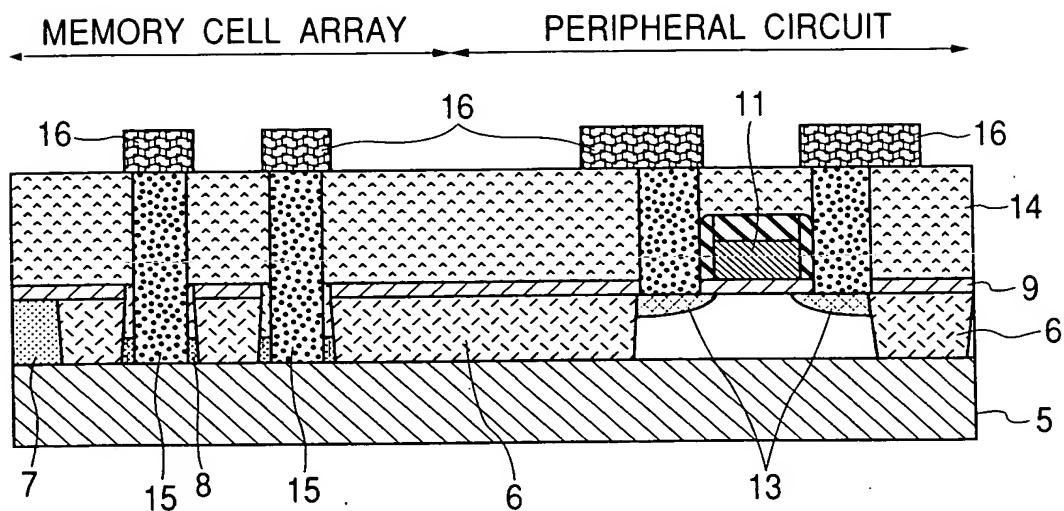
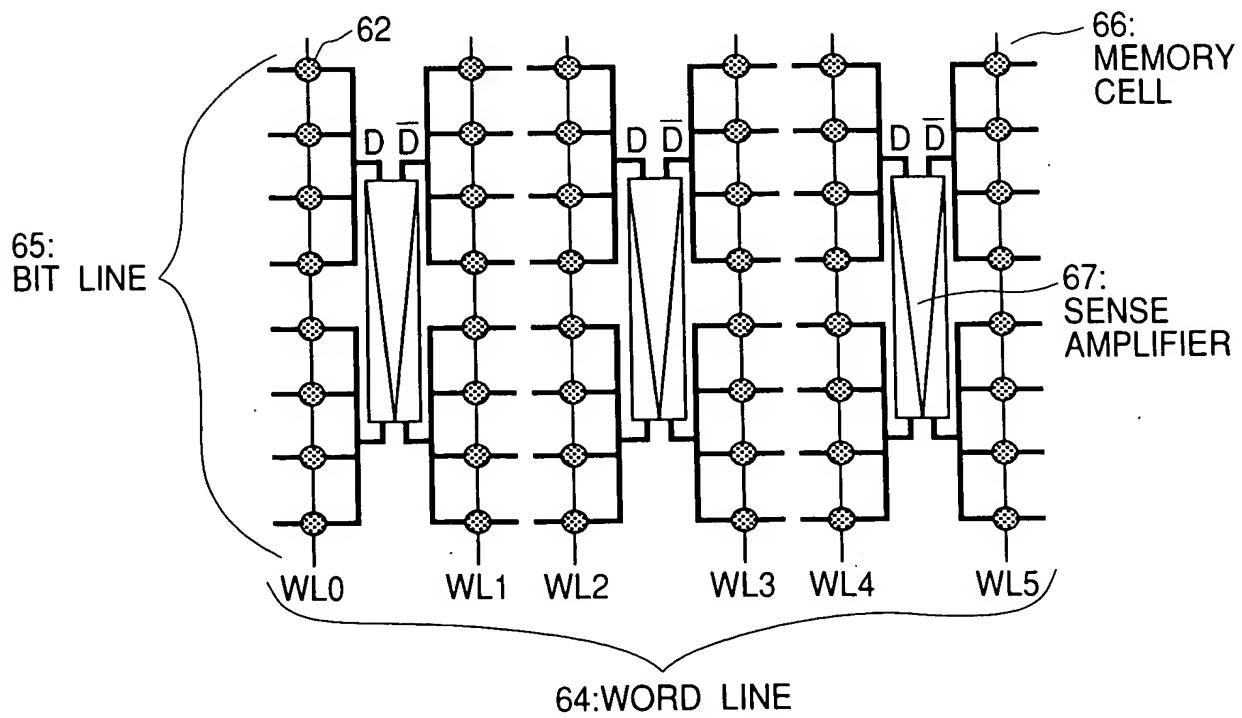
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**FIG. 32**

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**FIG. 33****FIG. 34**

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**FIG. 35****FIG. 36**

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FIG. 37

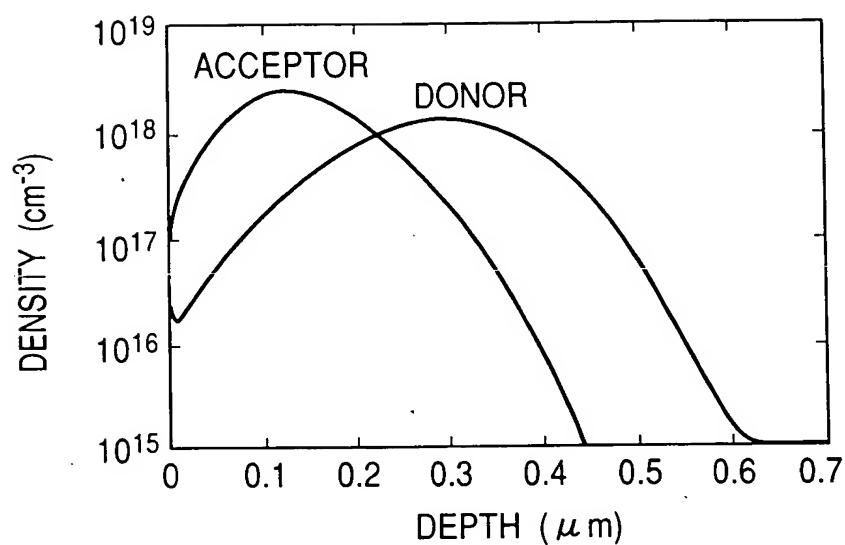
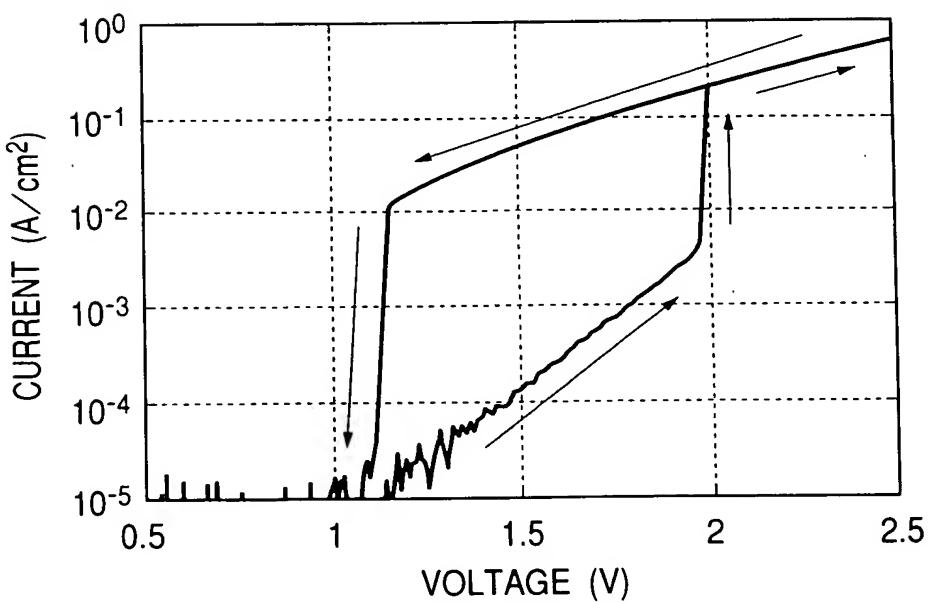


FIG. 38



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FIG. 41

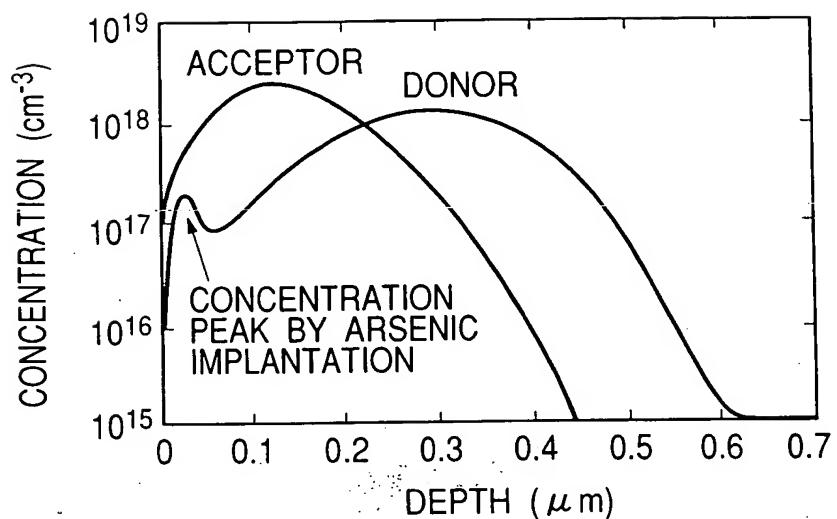
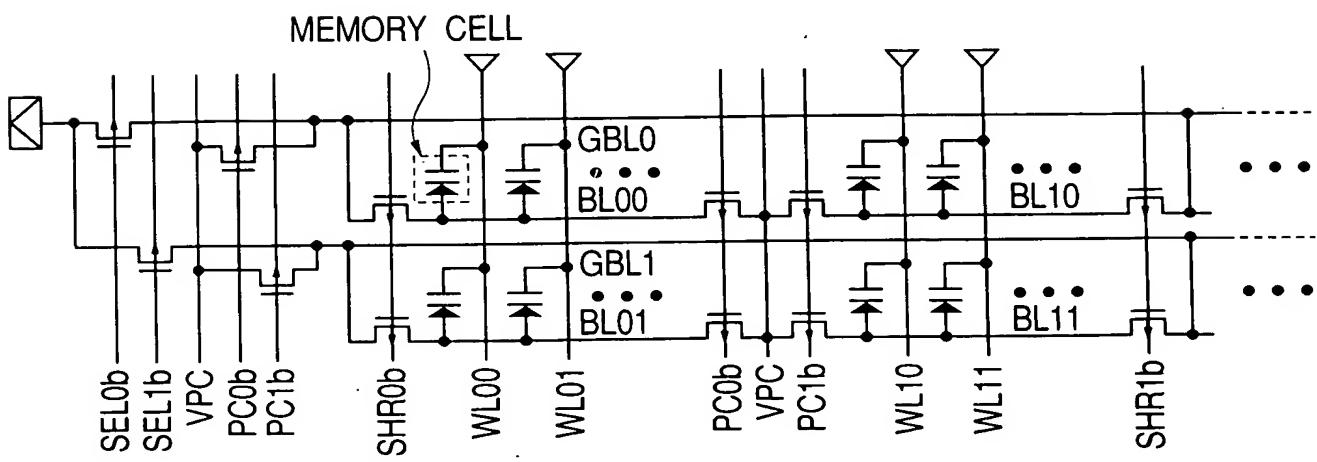


FIG. 42



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FIG. 39

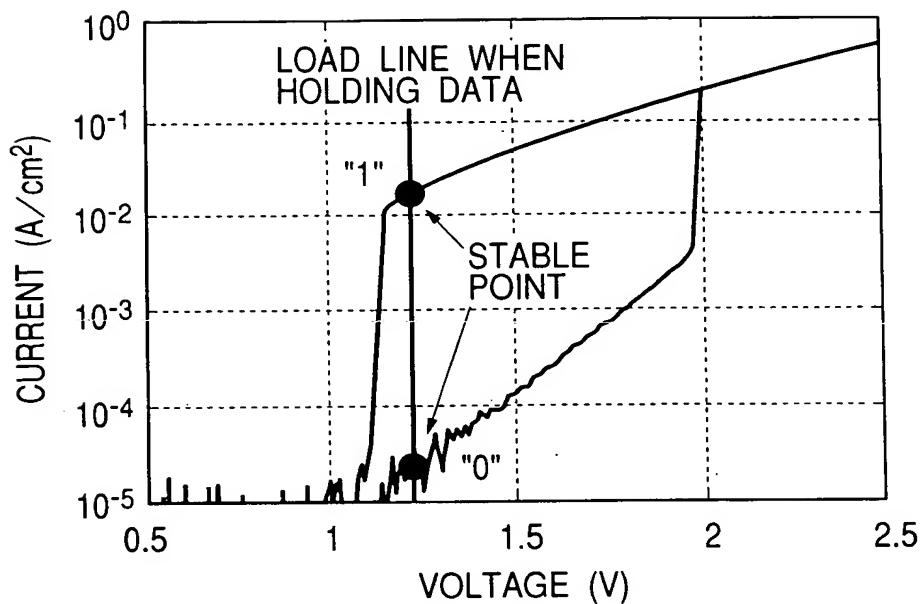


FIG. 40

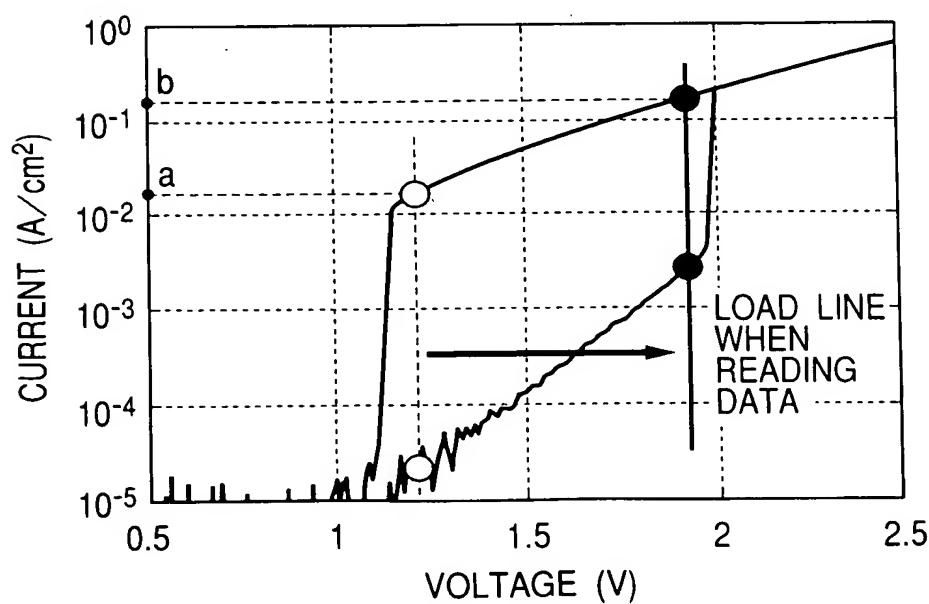


FIG. 43

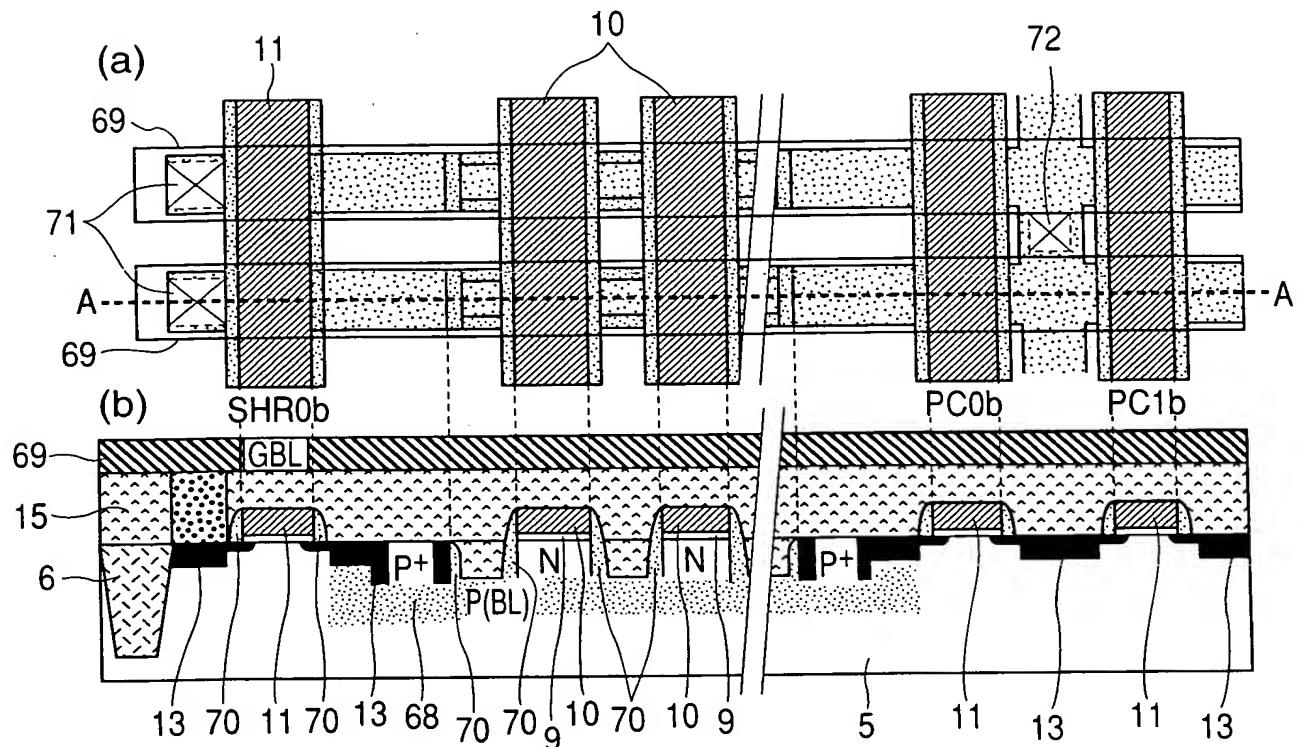


FIG. 44

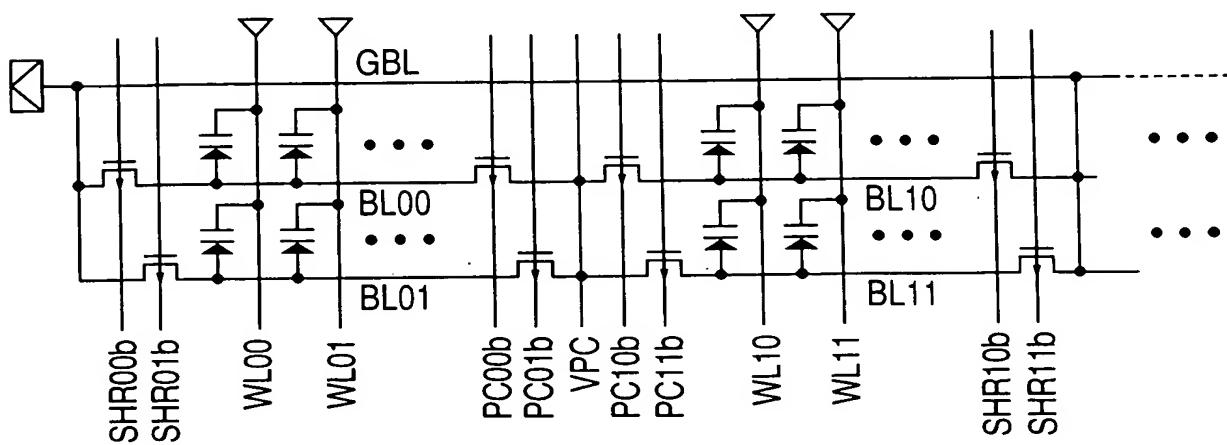
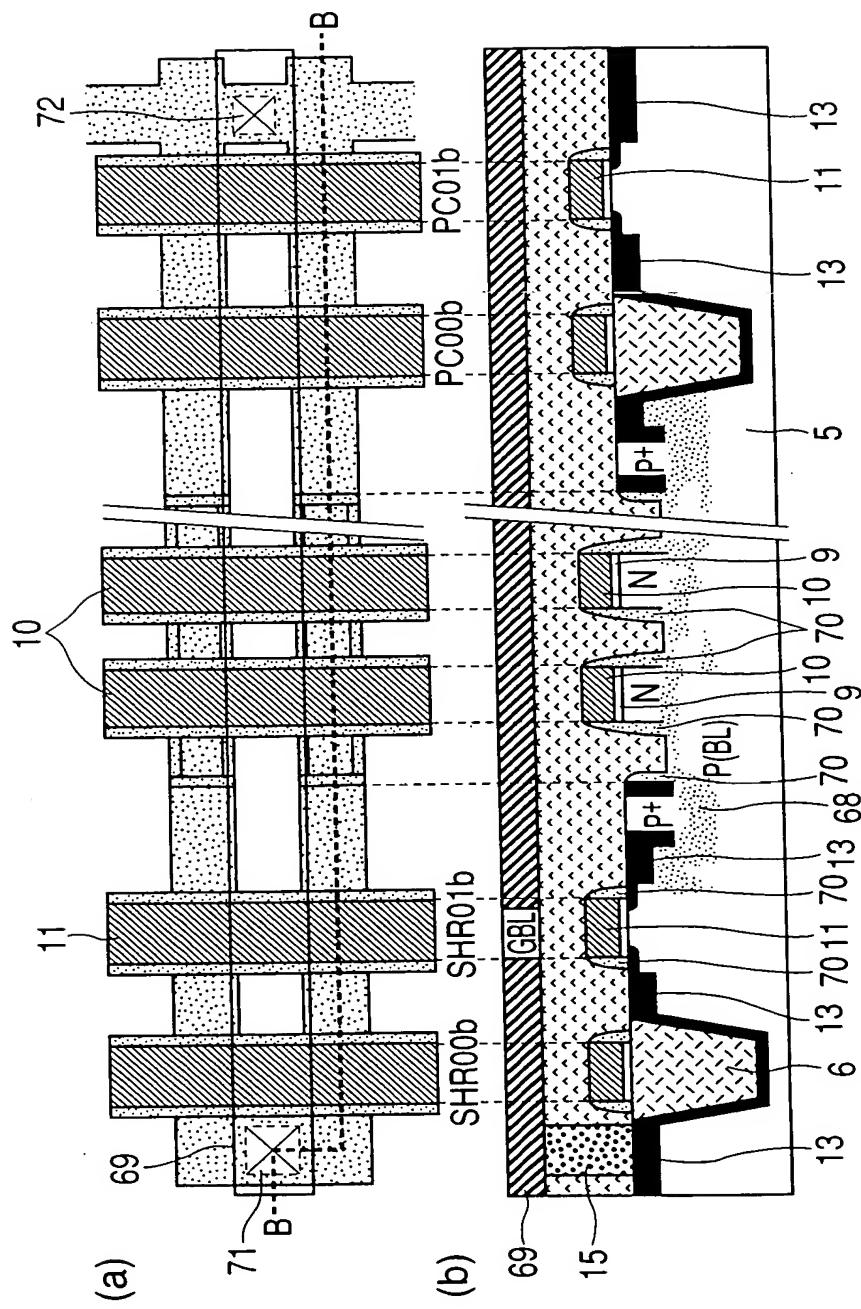


FIG. 45



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FIG. 46

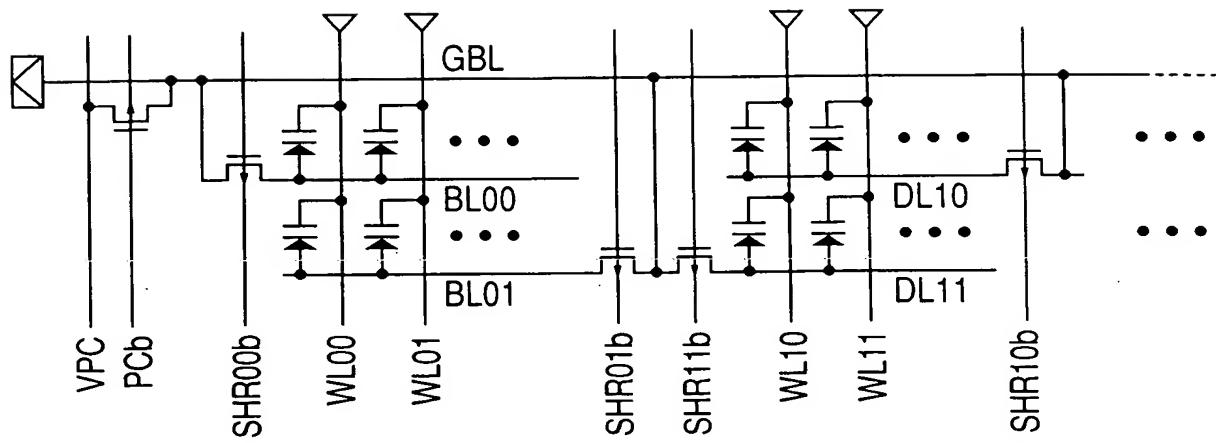


FIG. 47

